REMARKS

Status of the Claims

Claims 1-29 are pending.

Claims 1-29 have been rejected.

By this response, please **amend** claims 1, 4, 12, 15-19, 22-25, and **cancel** claims 5, 6, 20, 26, 27, 29.

Rejections

The Examiner rejected claims 1-8, 22-27 under 35USC103(a) as being anticipated by Goodman (US 2002/0073413) in view of Desikan et al.

Amended claim 1 includes the following features:

> a plurality of shared memory cells, each shared memory cell comprising a single non-volatile memory cell integrated with a single DRAM cell;
>
> a plurality of processor elements, each processor element being integrated with a shared memory cell, each processor elements accessing data from a corresponding shared memory cell that is integrated with the processor element, and performing processing on the data.

Support for the amendments can be found throughout the specification, and more specifically, on page 4, last paragraph, where it is stated "the non-volatile memory cells 110, 112, 114, 116 can be integrated with the processor elements 120, 122, 124, 126. As will be described, the non-volatile memory cells 110, 112, 114, 116 can be magnetic memory cells. An embodiment includes each magnetic memory cell 110, 112, 114, 116 being formed adjacent to a substrate, and the corresponding processor 120, 122, 124, 126 element being formed in the substrate adjacent to the magnetic memory cell." Page 8, fourth and fifth paragraphs, state " Figure 5 show a circuit schematic of an integrated

MRAM cell and DRAM cell according to an embodiment of the invention. The embodiment includes a **shared** DRAM/MRAM cell 500 that includes a first memory cell 510, and a non-volatile memory cell 520 that is interfaced to the first memory cell 510.

The first memory cell 510 can include a DRAM cell. The DRAM cell shown in Figure 5 includes a DRAM controlling transistor QD and a storage capacitor CD. Charge is both stored on the storage capacitor CD, and sensed from the storage capacitor CD through the word line WL and a bit line DBL."

Additionally, support is found on page 7, paragraphs 5 and 6, where it is stated "Figure 3 shows an MRAM cell 200 and processor element 340 according to an embodiment of the invention. The MRAM cell 200 as shown in Figure 3 is formed over a substrate 350. The substrate 350 can include a corresponding processor element 340.

As will be described, the structure shown in Figure 3 is desirable because the MRAM cell 200 does not include any transistor elements. Therefore, the MRAM cell can be formed during the conductor processing of an integrated circuit. That is, semiconductors within the substrate 350 typically include conductive lines formed over the substrate 350. The MRAM cell provides the advantage of being formed during the formation of the conductive lines. This provides ease of producing, and allows the MRAM cell 200 to be formed proximate to the corresponding processor element 340."

Figures 3-9 also provide support for the amended claims. That is, these figures show correspondence/integration between shared memory cells (non-volatile memory cells and DRAM cells) and processor elements.

Claim Rejections Under35USC103(a)

It is respectfully noted that to substantiate a *prima facie* case of obviousness the initial burden rests with the Examiner who must fulfill three requirements.

More specifically:

To establish a prima facie case of obviousness, three basic criteria must be met.

First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings.

Second, there must be a reasonable expectation of success.

Finally, the prior art reference (or references when combined) must teach or suggest all claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP Sec. 2143, *In re vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Paralleling the MPEP references cited above, the Federal Circuit has enunciated several guidelines in making a 35USC103 obviousness determination. A prima facie case of obviousness is established when and only **when the teachings from the prior art itself** would appear to have **suggested** the claimed subject matter to a person of ordinary skill in the art. *In re Bell,* 991 F.2d 783, 26 U.S.P.Q.2d 1529, 1531 (Fed Cir. 1993) (quoting *In re Rinehart*, 531 F.2d 1048, 1051 (C.C.P.A. 1976)). (Emphasis added). "The mere fact that the prior art **may** be modified in the manner suggested by the Examiner does **not** make the modification obvious unless the prior art suggested the desirability of the modification." (Emphasis added) In re Fritch, 23 USPQ 2d 1780, 1783-84 (Fed. Cir. 1992).

Goodman provides a multi-node processing network system with a plurality of processors 105 coupled in a network 106, together with a master source 108. As illustrated in FIG. 1, the processors 105 each comprise a processor interface 112 coupling the processor in the network, a non-volatile memory 113, such as a ROM, for storing code comprising at least a boot program, a processor memory 114, such as a high speed

RAM, storing a code image providing a fully operational state of the processor, and a processing unit 115 couple to the non-volatile memory 113, the processor memory 114 and the processor interface 112.

The processors 105 of Goodman are connected to the non-volatile memory 113 through an interface 112. Goodman does not teach any type of non-volatile memory/DRAM cell correspondence or integration with any particular processor.

The claimed invention includes a plurality of processor elements, each processor element being integrated with a shared memory cell, each processor elements accessing data from a corresponding shared memory cell that is integrated with the processor element, and performing processing on the data.

The claimed inventions allows for the benefits described in the specification in the sixth paragraph of page 7. More specifically, "the structure shown in Figure 3 is desirable because the MRAM cell 200 does not include any transistor elements. Therefore, the MRAM cell can be formed during the conductor processing of an integrated circuit. That is, semiconductors within the substrate 350 typically include conductive lines formed over the substrate 350. The MRAM cell provides the advantage of being formed during the formation of the conductive lines. This provides ease of producing, and allows the MRAM cell 200 to be formed proximate to the corresponding processor element 340."

Goodman includes separate (not integrated) processor and memory elements. Goodman does not provide any suggestions for integration, any embodiments adaptable for integration, nor does Goodman provide any suggestion for the advantages of integration. Goodman does not provide any discussion the advantages obtained by specifying the proximity of corresponding processor elements and memory elements.

The Examiner stated that Desikan teaches integration of processors with non-volatile memory cells. Desikan states that "MRAM devices ..... can be integrated into the processor die in layers above those of conventional wiring." Desikan does not

provide any teaching of structures allowing integration of MRAM and non-volatile memory. Such integration is not taught or obvious in light of Desikan.

Goodman and Desikan do not provide for shared memory cells in which each shared memory cell includes a single non-volatile memory cell integrated with a single DRAM cell. Desikan teaches MRAM as a replacement for DRAM. Therefore, Desikan teaches away from integrating MRAM, DRAM and a processor element. Goodman and Desikan in combination do not provide for a processor element being integrated with a shared memory cell.

Amended claim 1 is patentable over the cited prior art. Claims 2-21, 24-29 are directly or indirectly dependent on claim 1. Therefore, claims 2-4, 7-19, 21-25, 28 are patentable over the prior art.

Regarding amended claim 24, features of a structure are now included that the cited references do not come close to suggesting or making obvious. Support for the features are found on Figures 5 and 6, and within the supporting descriptions of Figures 5 and 6.

The Examiner rejected claims 9-21 under 35USC103(a) as being unpatentable over Goodman and Desikan in view of Young (5,621,683).

Claims 9-20 are directly or indirectly dependent on claim 1. Therefore, claims 9-20 are patentable. However, claims 9-20 include additional features that make them further patentable over the cited prior art.

Young teaches a semiconductor memory element comprising a non-volatile memory transistor as a driver transistor and having an adequate difference in output signal from the cell for the different states of the memory transistor to permit the assembly of a large number of such memory cells in an array (column 2, lines 27-36). Reference is made to other thin film circuitry that may perform a logic-function and/or may comprise an active-matrix liquid-crystal display or other flat panel display and/or an image sensor.

Young does not include any suggestions of each processor elements accessing data from a corresponding non-volatile memory cell that is most proximate to the processor element, and performing processing on the data. Young makes no reference of the relative proximity of processor elements and non-volatile memory cells, or the processing of data within non-volatile memory cells. Regarding claim 9, Young makes no suggestions regarding any correspondence between an image sensor and each of the magnetic memory cells. New claim 28 additionally includes the image sensor corresponding with a magnetic memory cell is the image sensor most proximate to the magnetic memory cell. New claim 29 additionally includes the display pixel corresponding with a non-volatile memory cell is the display pixel most proximate to the non-volatile memory cell.

Claim 13 is additionally patentable over the cited prior art because claim 13 includes the features wherein each image sensor is formed adjacent to a corresponding non-volatile memory element, and each non-volatile memory element is formed adjacent to a substrate, the substrate comprising a corresponding processor element formed adjacent to the non-volatile memory element. Young does not break the image sensors down to a one to one correspondence with non-volatile memory elements and processor elements.

Claim 14 is additionally patentable over the cited prior art because claim 14 includes the features wherein each image sensor is formed adjacent to a corresponding non-volatile memory element, and each non-volatile memory element is formed adjacent to a substrate, the substrate comprising a corresponding processor element and DRAM cell formed adjacent to the non-volatile memory element. Young does not break the image sensors down to a one to one correspondence with the non-volatile memory cells, processor elements and DRAM cells. Claim 21 is patentable for similar reasons.

Amended claim 19 includes the features of a display pixel receives image data from a non-volatile memory element, and wherein the display pixel is an LED and a bias current of the LED is dependent upon a resistance of the non-volatile memory element. Young teaches a very general association between memory and display devices. Young

does not provide any correspondence between LEDs and memory elements. Additionally, Young does not provide any teachings of how LEDs are biased based upon connections with the memory, or how the memory accomplishes the biasing.

Independent claims 22, 23 include similar features as claim 1. Therefore, claims 22, 23 are patentable over the prior art.

No new matter has been added by these amendments.

The applicants respectfully request reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,
Manish Sharma

By: Brian Short
Brian Short, Attorney for Applicants
Reg. No. 41,309
Date: July 28, 2005
Ph. No.: 650-236-4890

Hewlett-Packard Company
Intellectual Property Section
1501 Page Mill Rd. M/S 1197 (4U-10)
Palo Alto, CA 94304-1112